CLAIMS

What is claimed is:

1. A high current, multi-phase voltage multiplier, comprising:

a multiple phase active level overlapping clock generator that generates multiple pairs of phase clocks, each of the pairs of phase clocks having an active portion and an inactive portion, the inactive portions of one of each of the pairs of phase clocks never overlapping; and

a plurality of voltage divider pairs, each of the voltage dividers formed by the junction of an input end switch and an output end switch, wherein each of the voltage dividers provides a switch control signal to the other of two voltage dividers in the pair, each of the voltage dividers being coupled to a charging capacitor, the charging capacitor being driven by the multiple phase active level overlapping clock generator.

2. The voltage multiplier of Claim 1, wherein the clock generator provides a phase clock signal unique to each voltage divider.

3. The voltage multiplier of Claim 2, wherein the phase clock signal is buffered between the clock generator and its corresponding charging capacitor.

4. The voltage multiplier of Claim 1, wherein the input end switch and the output end switch of each of the plurality of voltage divider pairs are transistors.

5. The voltage multiplier of Claim 4, wherein the transistors are bipolar transistors.

6. The voltage multiplier of Claim 4, wherein the transistors are field effect transistors.

7. The voltage multiplier of Claim 6, wherein the input end switch is an N type metal oxide semiconductor field effect transistor (NMOS FET) and the output end switch is a P type metal oxide semiconductor field effect transistor (PMOS FET).

8. The voltage multiplier of Claim 7, wherein the NMOS and PMOS FETs of each of the voltage dividers are electrically connected together through their drain terminals.

9. The voltage multiplier of Claim 8, wherein the output of the voltage multiplier is provided through the source terminals of the PMOS transistors of the plurality of voltage dividers.

10. The voltage multiplier of Claim 9, wherein the source terminals of the PMOS transistors are tied together.

11. The voltage multiplier of Claim 10, wherein the output of the voltage multiplier is smoothed by a smoothing capacitor that capacitively couples the output to circuit ground.

12. The voltage multiplier of Claim 11, wherein the output of the voltage multiplier is filtered.

13. The voltage multiplier of Claim 12, wherein the filter includes an inductor through which the output passes.

14. The voltage multiplier of Claim 1, wherein the clock generator includes a counter that is clocked by a basic external clock.

15. The voltage multiplier of Claim 14, wherein the clock generator includes a means for determining duty cycle.

16. The voltage multiplier of Claim 15, wherein the clock generator includes tapped delay circuitry.

17. A method for multiplying a voltage in a circuit, comprising:

setting a length of a phase clock period;

setting a duty cycle of the phase clock period;

pairing overlapping phase clock signals from all of a plurality of phase clock signals; and

charging and discharging capacitors associated with each phase clock pair.

18. The method of Claim 17, wherein the plurality of phase clock signals are four or more in number.

19. The method of Claim 18, wherein each of the capacitors is involved in the operation of two voltage dividers.

20. The method of Claim 19, wherein each of the capacitors controls switching of switches forming one of the two voltage dividers.

21. A high efficiency, high current multiphase voltage multiplier, comprising:

means for generating a plurality of unique phase clocks, the plurality of unique phase clocks being arranged into M pairs such that at least one phase clock of each pair is at an active HIGH level at any time, wherein M is an integer greater than 1;

means for multiplying a voltage; and

means for charging and discharging points of the means for multiplying a voltage.

22. The voltage multiplier of Claim 21, wherein the means for multiplying a voltage doubles the voltage.

23. The voltage multiplier of Claim 22, wherein the means for multiplying a voltage includes means for dividing a voltage.

24. The voltage multiplier of Claim 23, wherein the means for dividing a voltage includes means for switching.